

D

Model Name:GA-F2A58M-DS2


Component value change history

Version: 3.0
P-Code: U98126-0

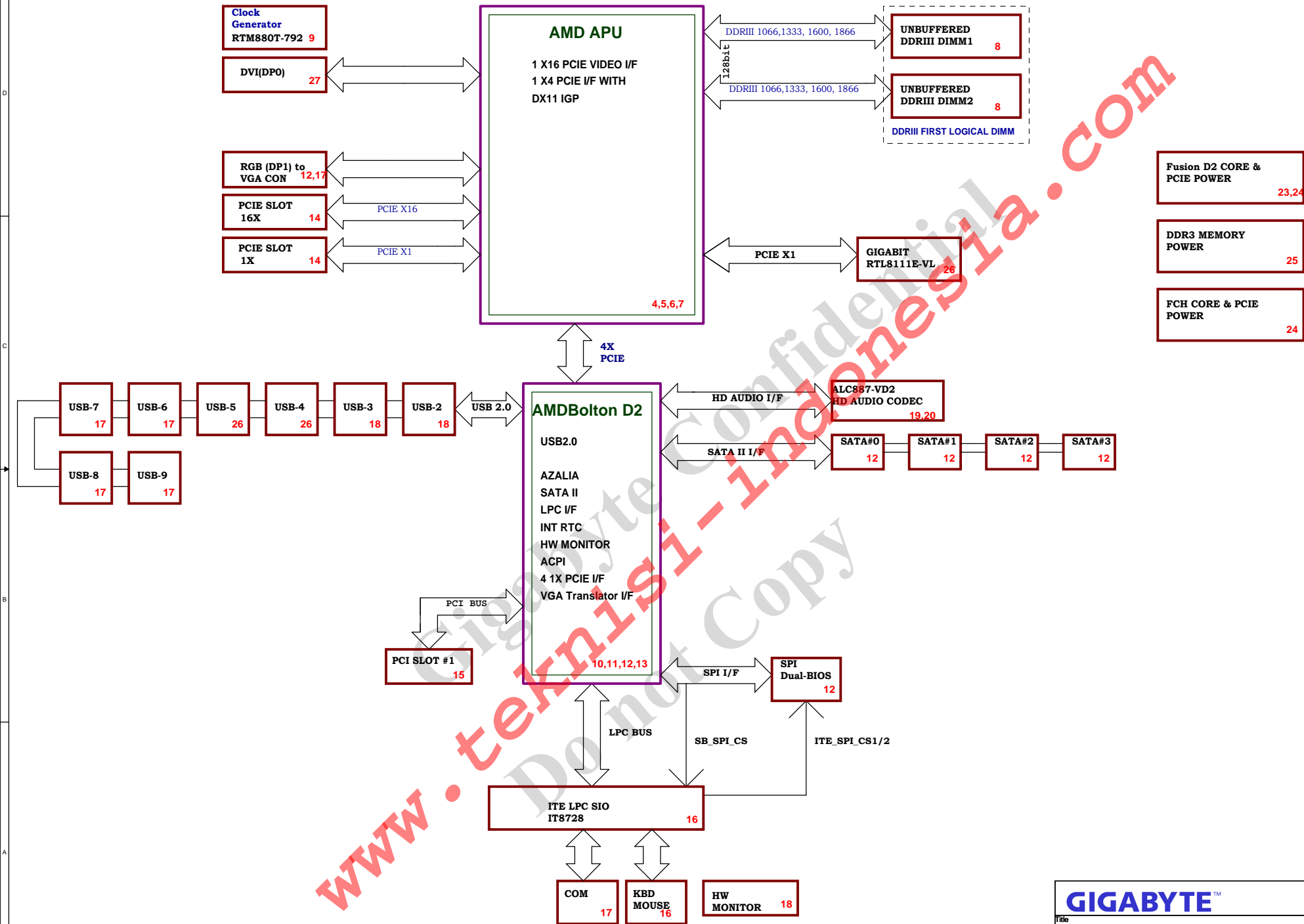
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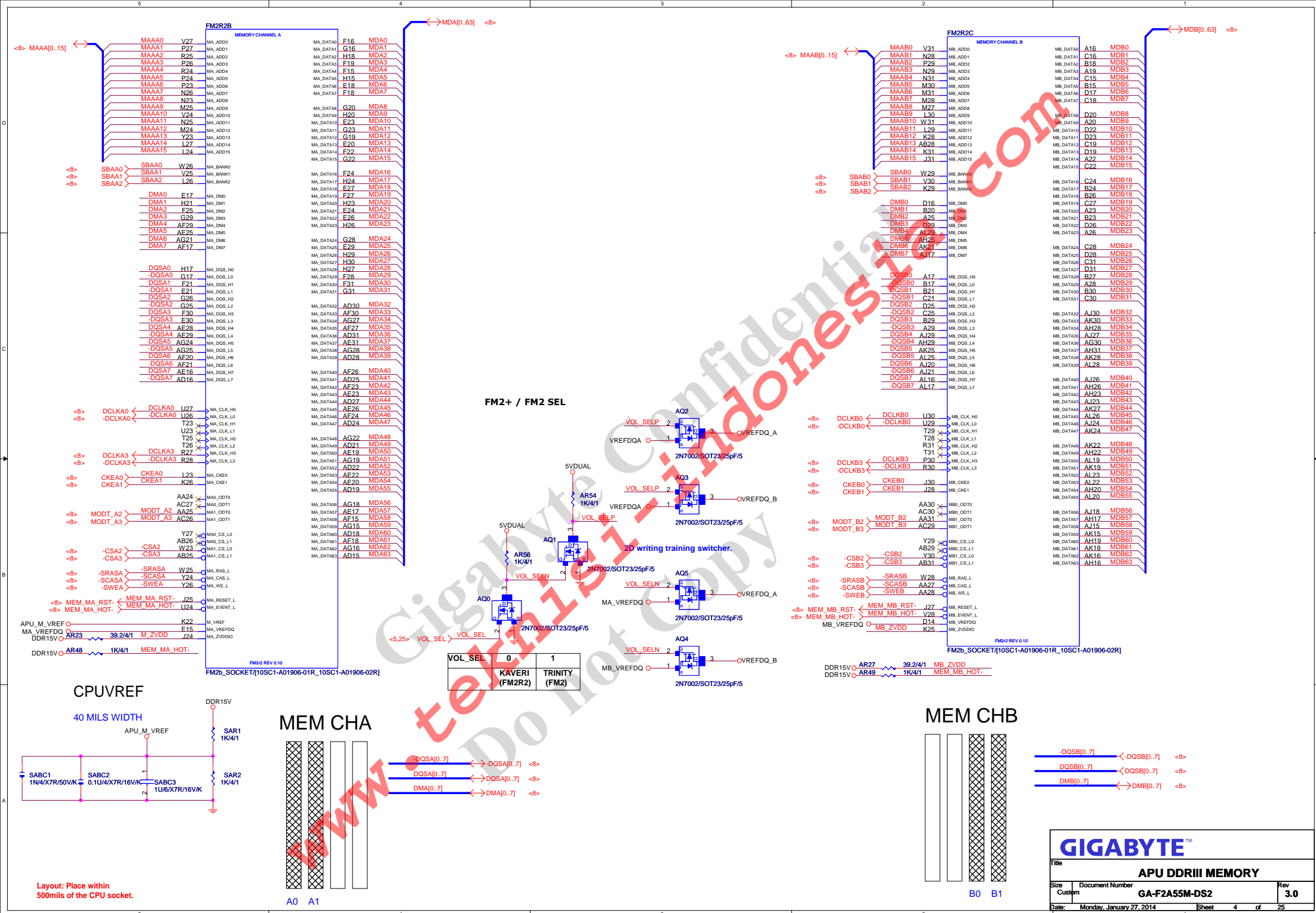
Circuit or PCB layout change for next version

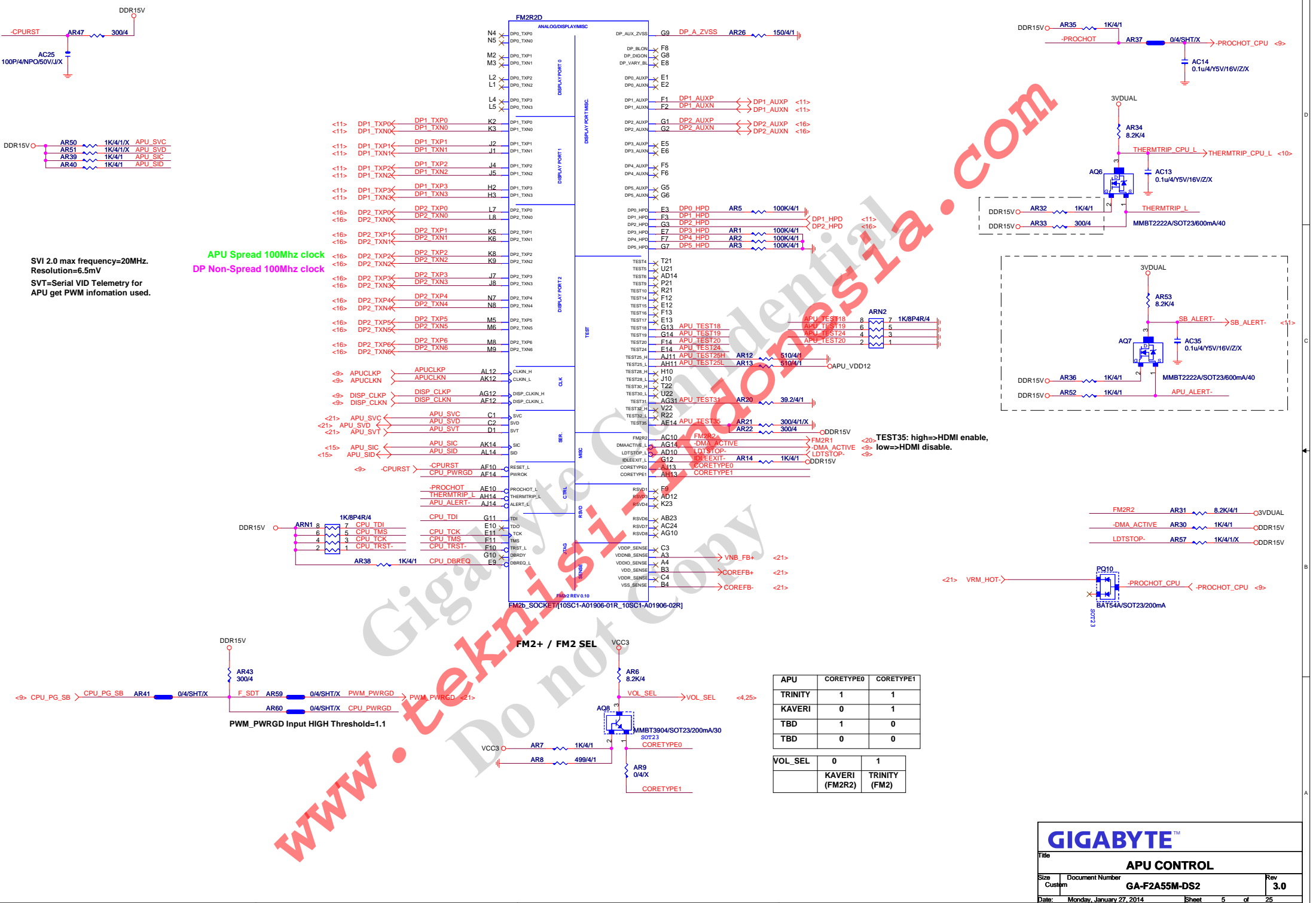
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Title				
BOM & PCB HISTORY				
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AMD Fusion Hudson CUSTOMER DESKTOP REFERENCE DESIGN







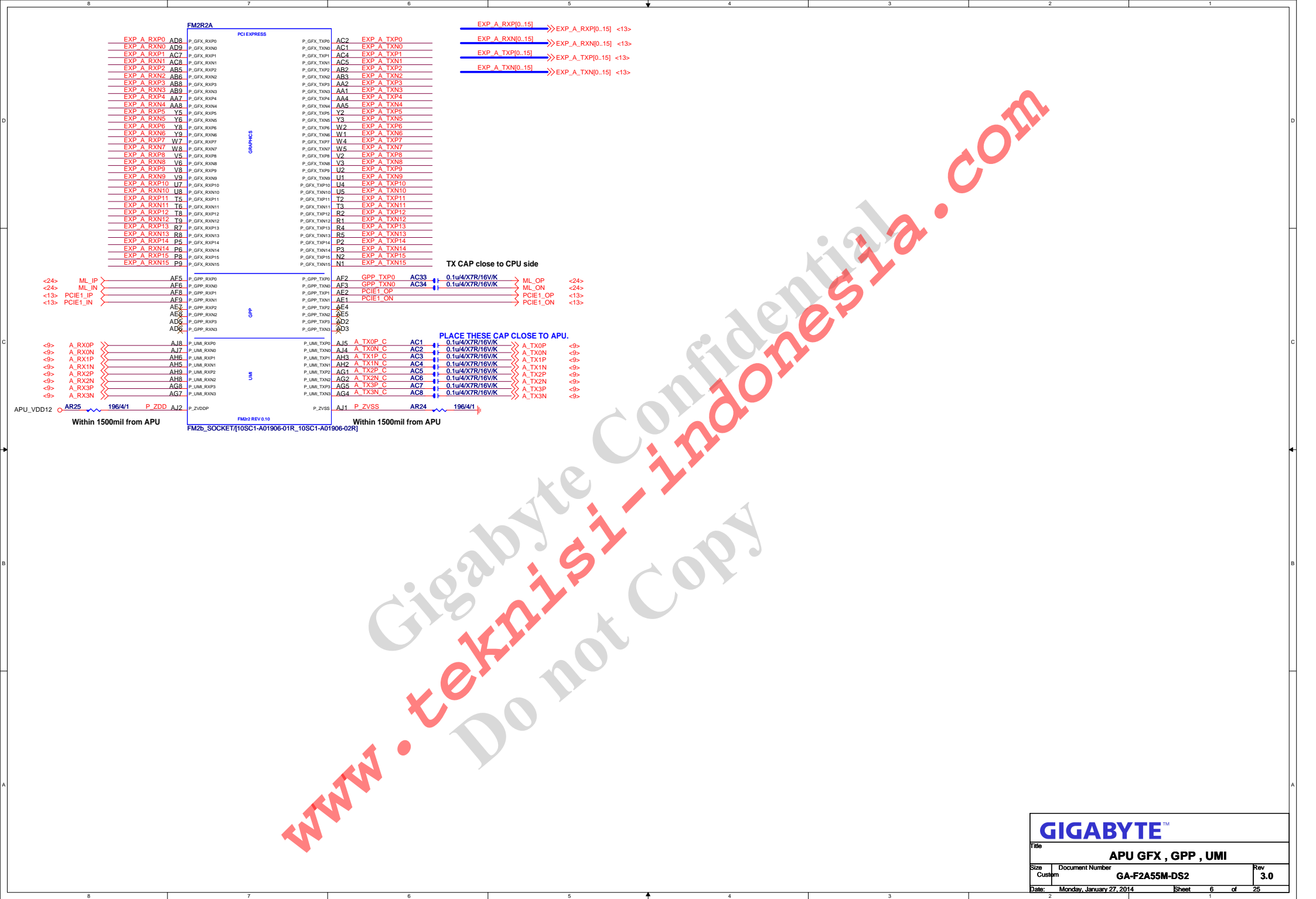
SVI 2.0 max frequency=20MHz.
Resolution=6.5mV
SVT=Serial VID Telemetry for
APU get PWM information used.

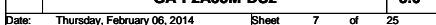
APU Spread 100Mhz clock
DP Non-Spread 100Mhz clock

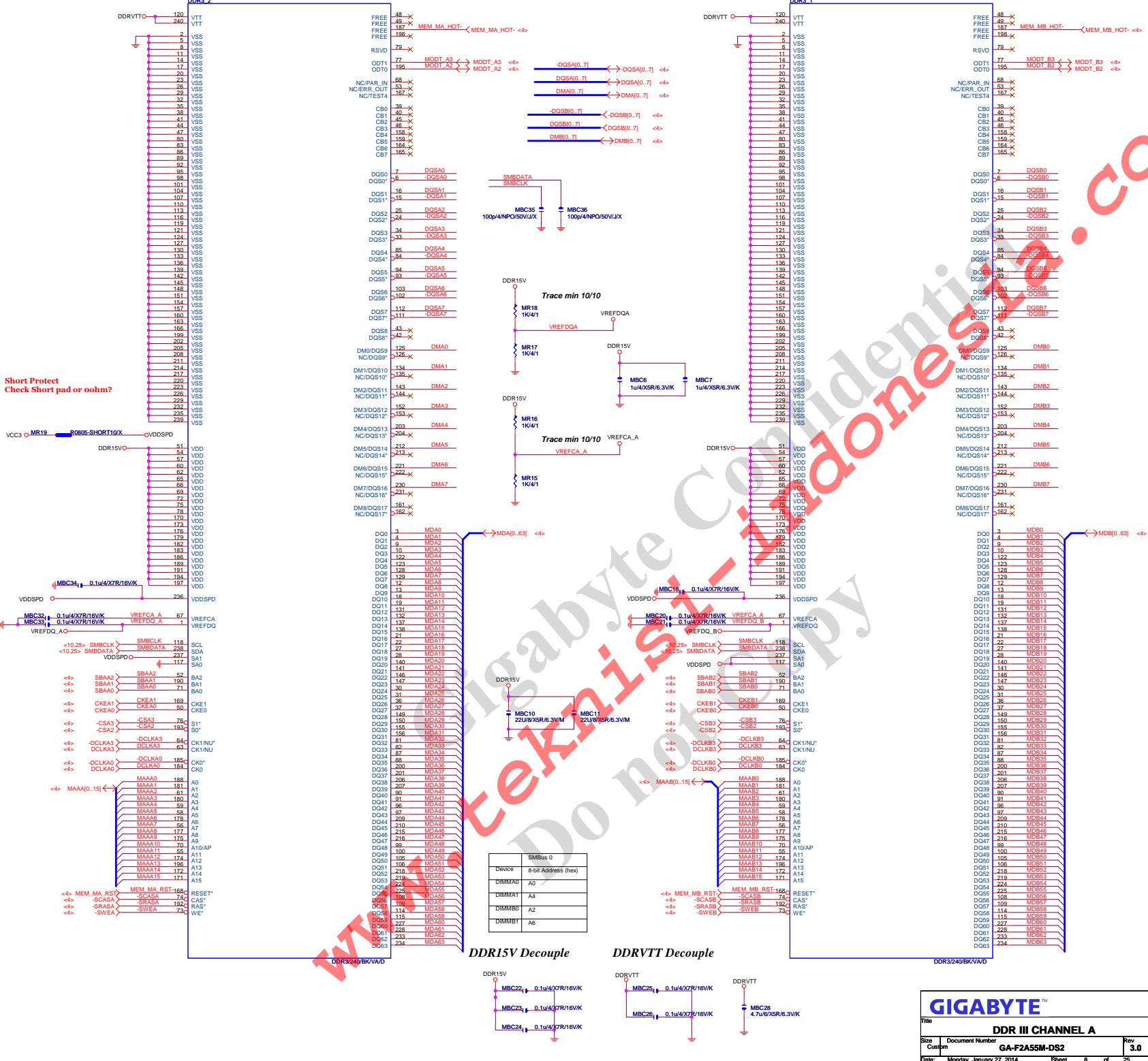
TEST35: high=>HDMI enable,
low=>HDMI disable.

APU	CORETYPE0	CORETYPE1
TRINITY	1	1
KAVERI	0	1
TBD	1	0
TBD	0	0

VOL_SEL	0	1
	KAVERI (FM2R2)	TRINITY (FM2)



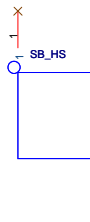




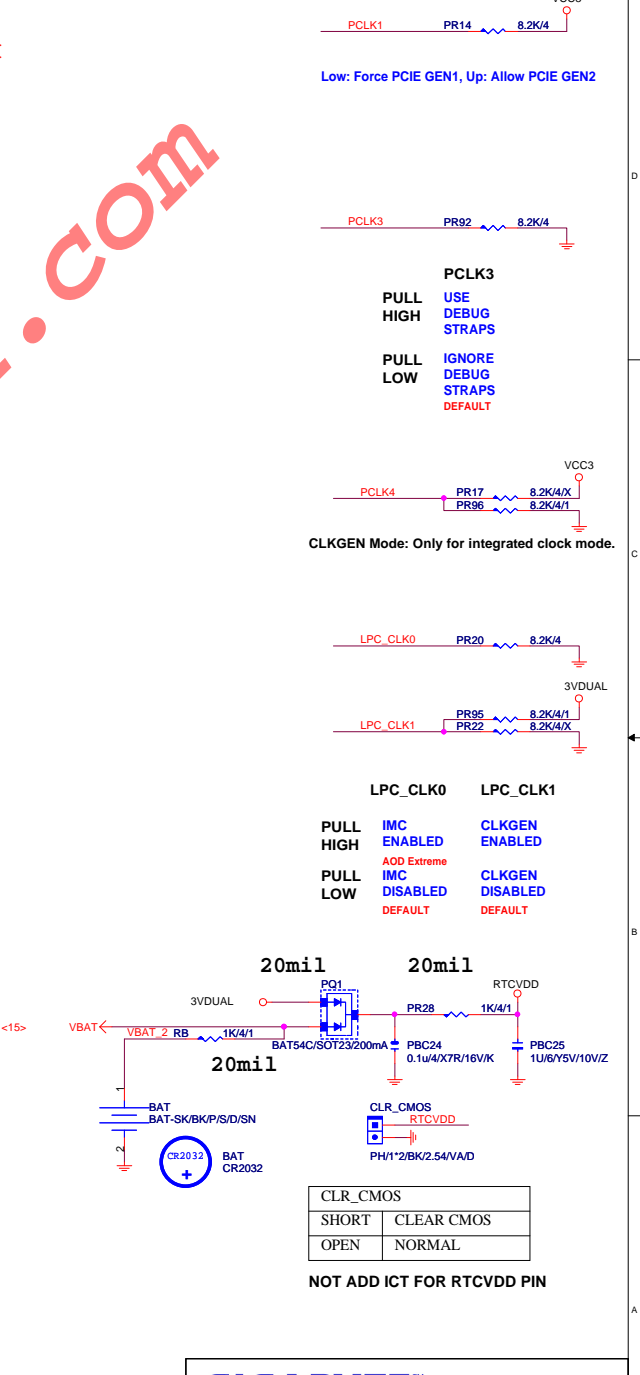
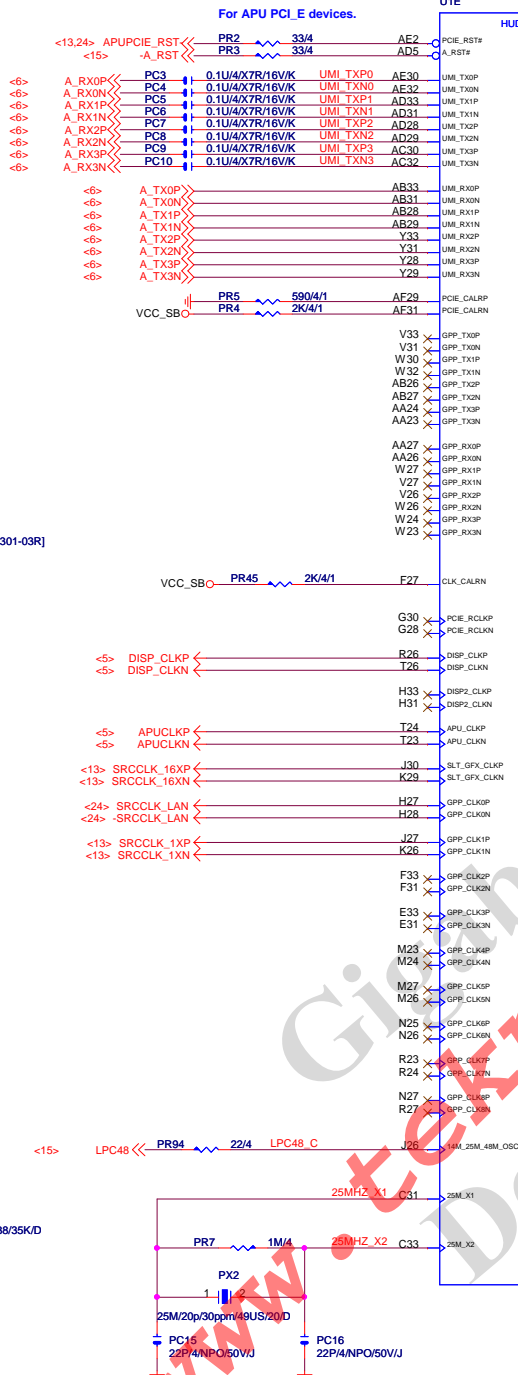
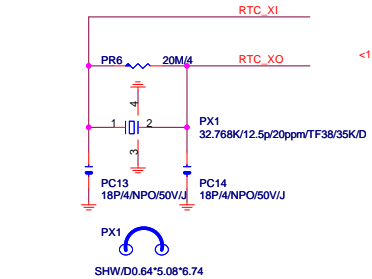


PLACE THESE PCIE AC COUPLING CAPS CLOSE TO SB850

S.B HEATSINK



SB_HS[12SP2-SA0301-01R_12SP2-SA0301-02R_12SP2-SA0301-03R]



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Hudson D3 PCIE/PCI/CPU/LPC

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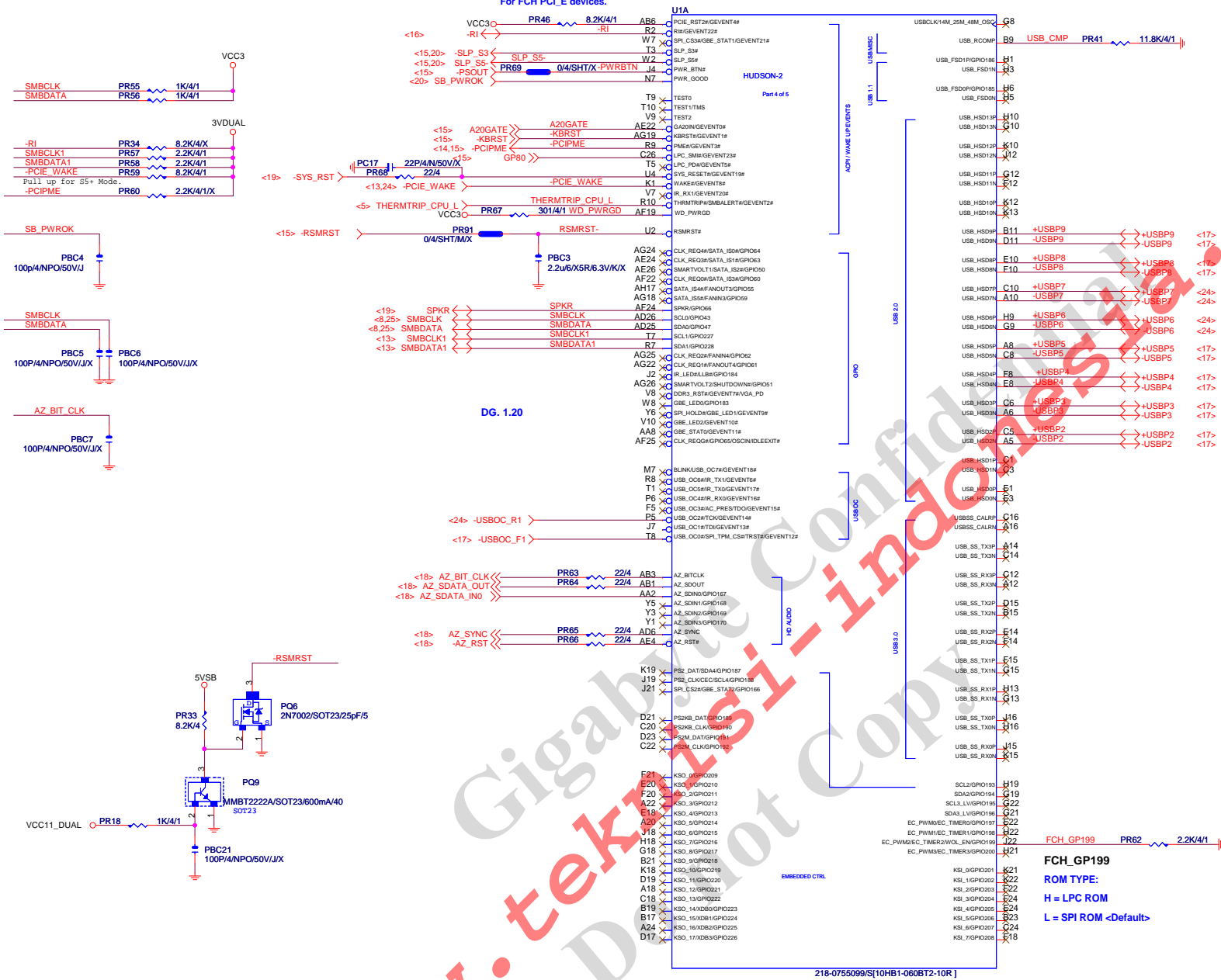
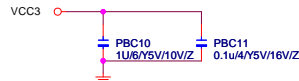


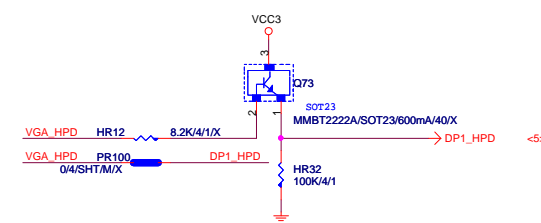
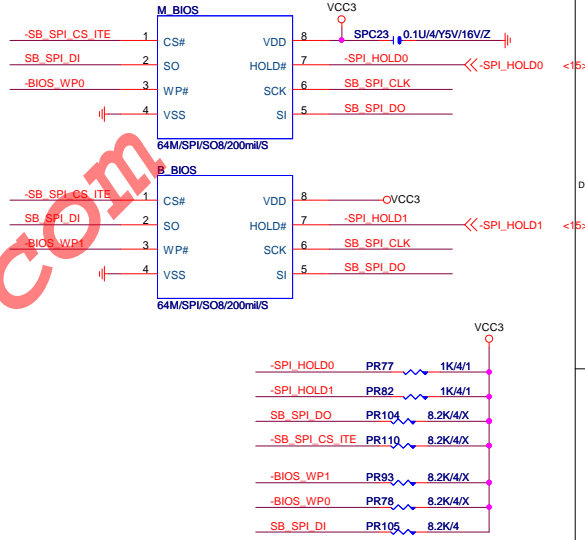
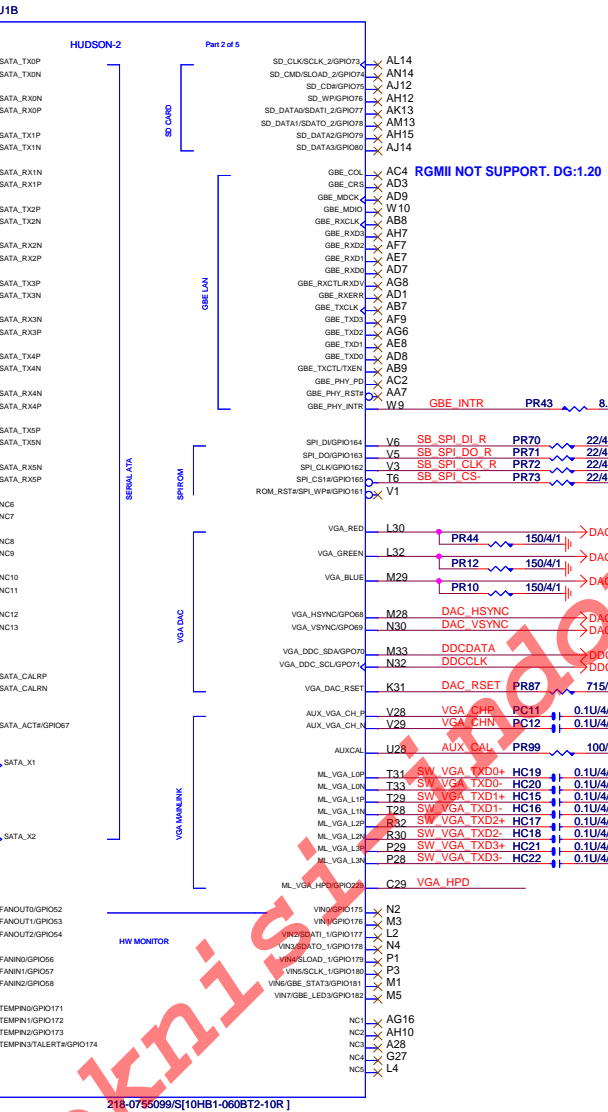
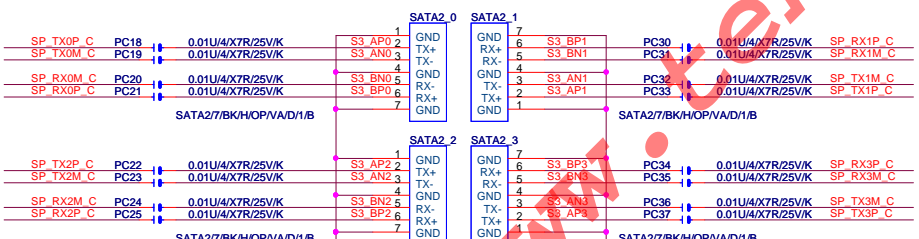
FIG. 1.20

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SATA 6-7 for Hudson D4.

PLACE SATA_CAL RES VERY CLOSE TO BALL OF U1



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TitleHudson D3 SATA/HWM/SPI

SizeCustomDocument NumberGA-F2A55M-DS2Rev3.0

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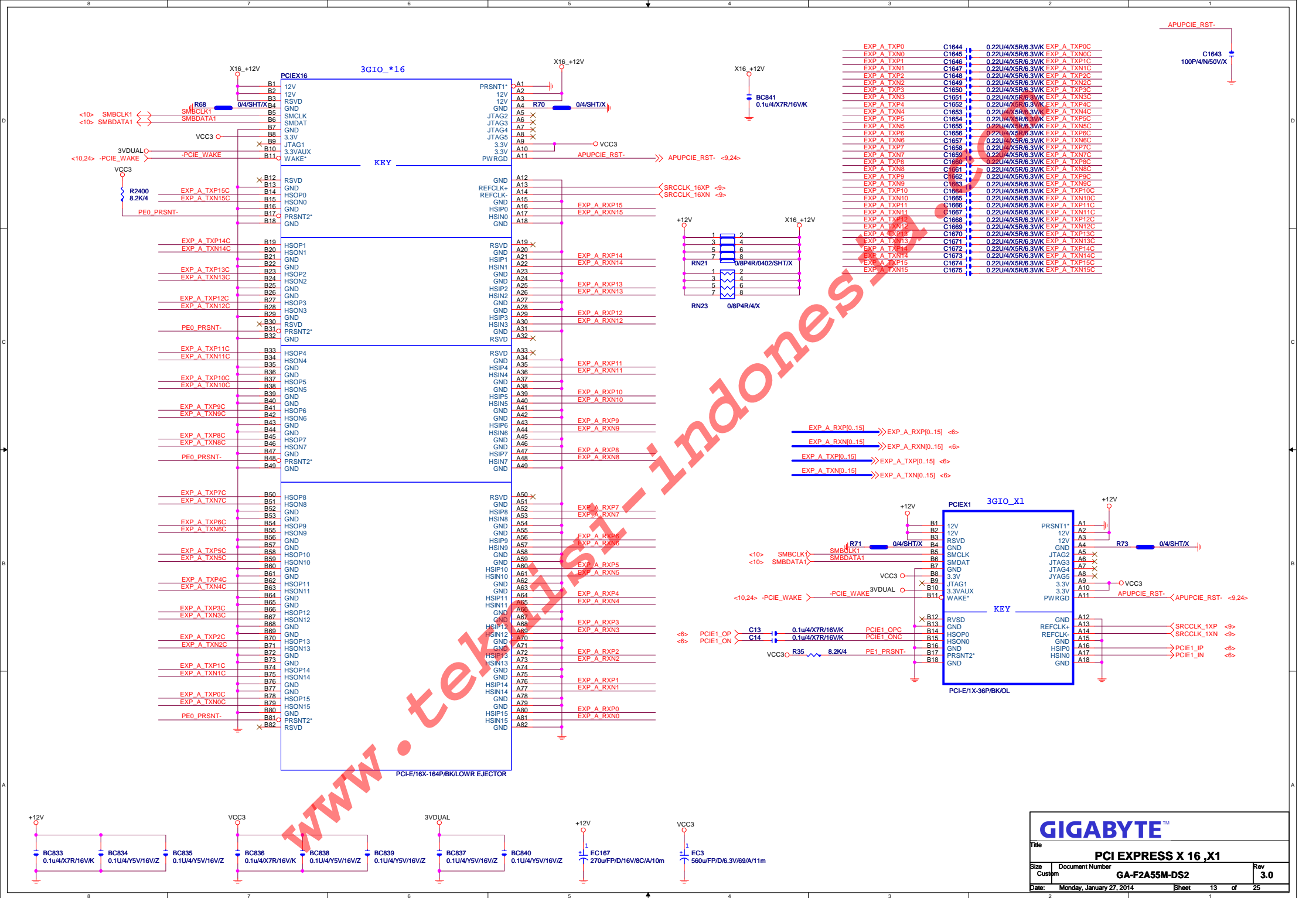
PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

Hudson 3/4 does not support an RGMII/MII interface.

218-0755099/S[10HB1-060BT2-10R]

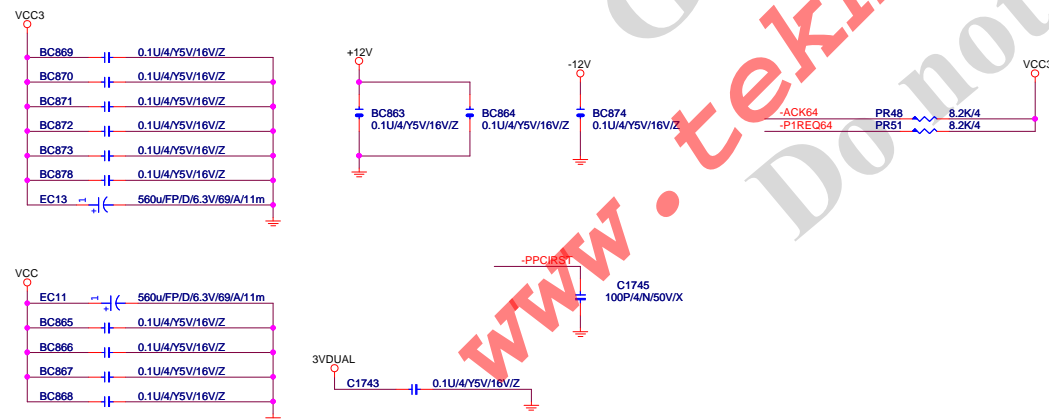
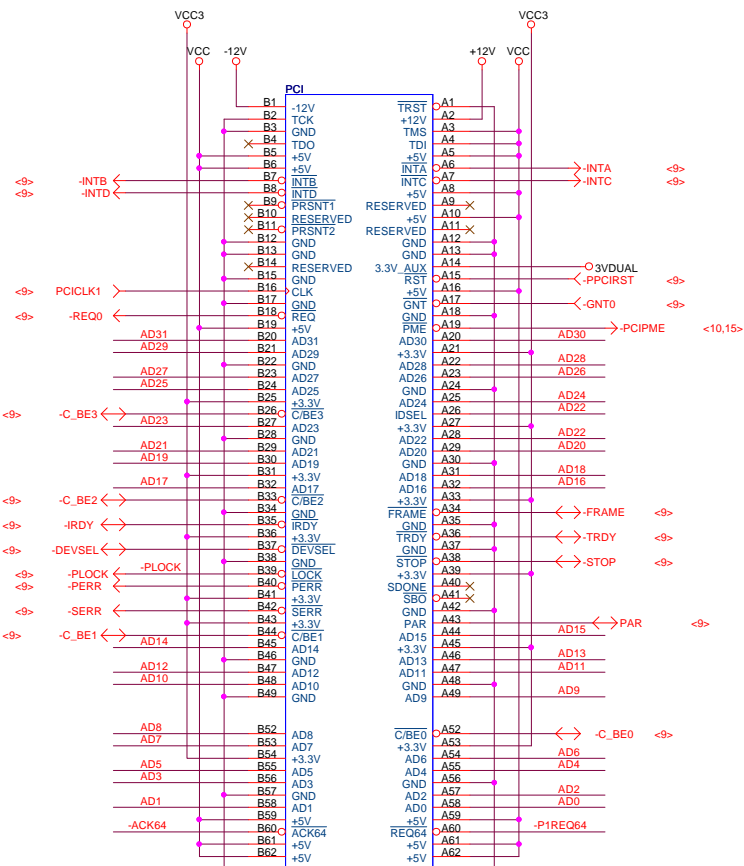
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Title		
HUDSON D3 PWR & GND		
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PCI SLOT 1,2

<9> AD[0..31] <-> AD[0..31]

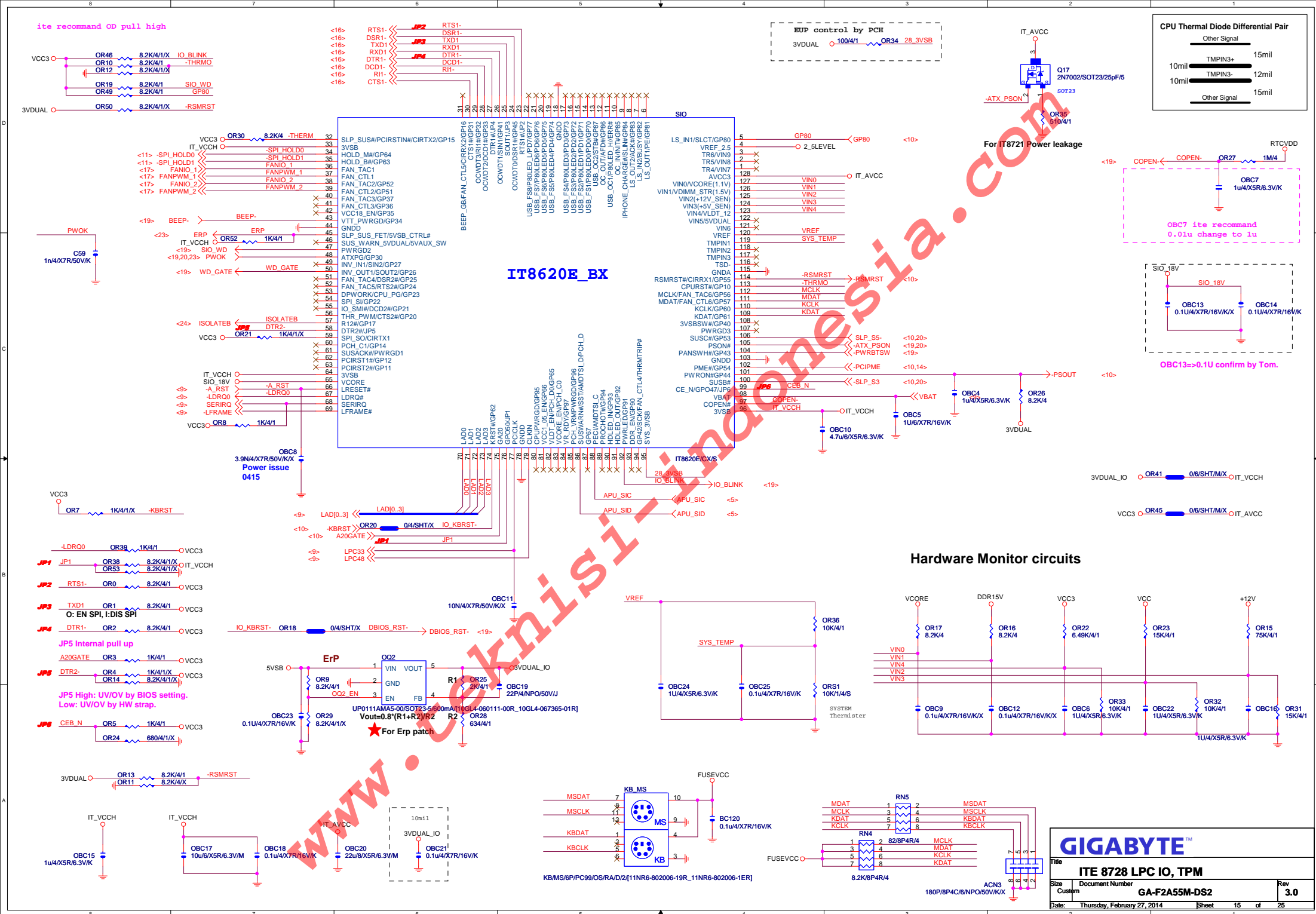


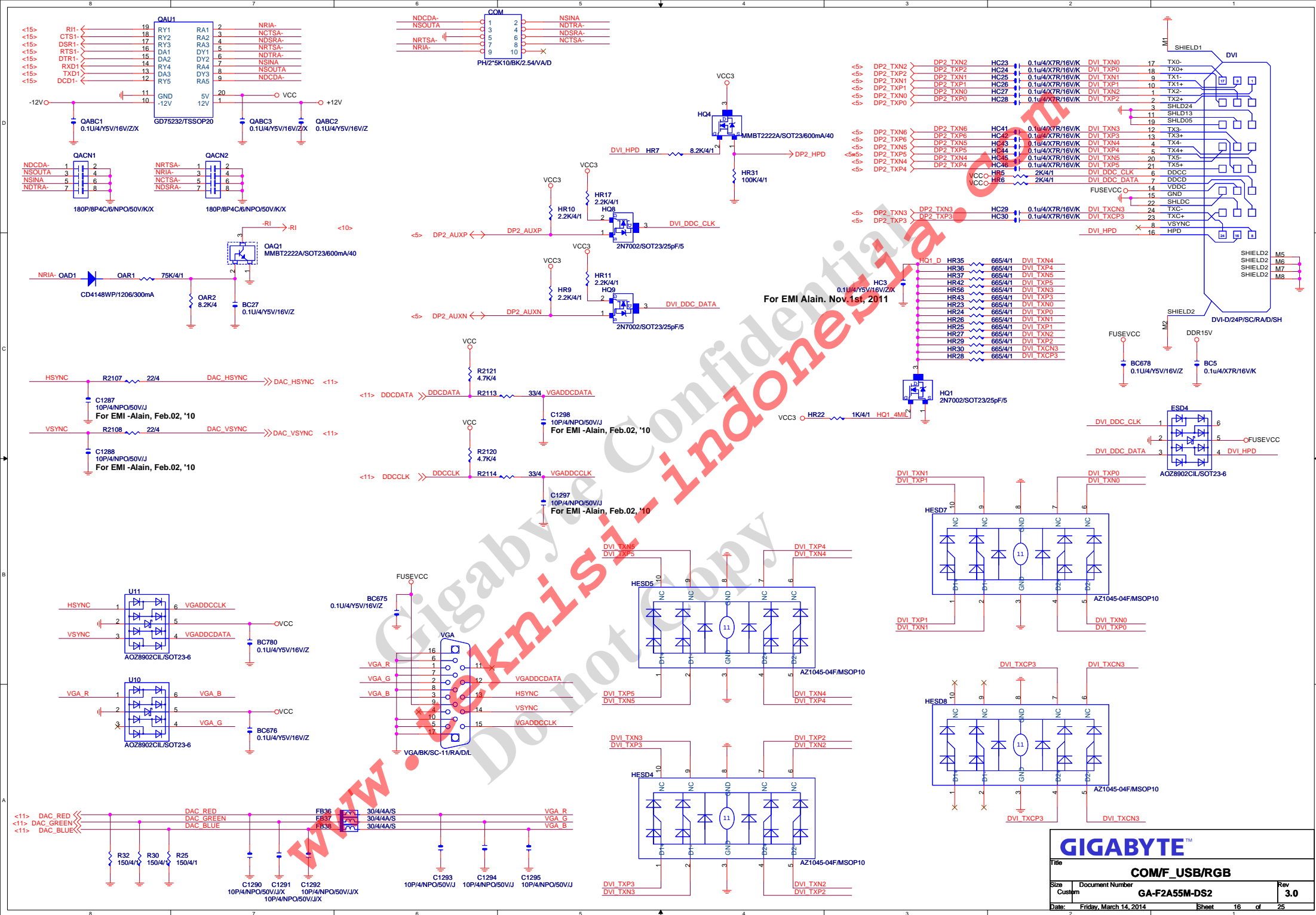
GIGABYTE

Title **PCI SLOT**

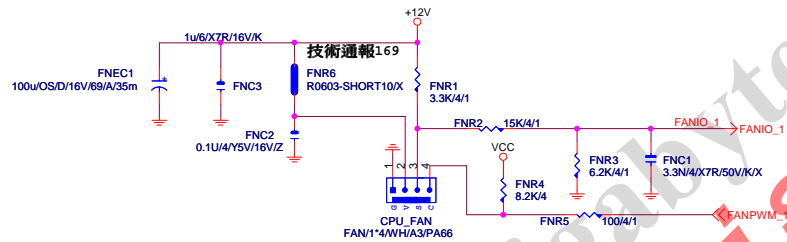
Size Custom Document Number **GA-F2A55M-DS2** Rev **3.0**

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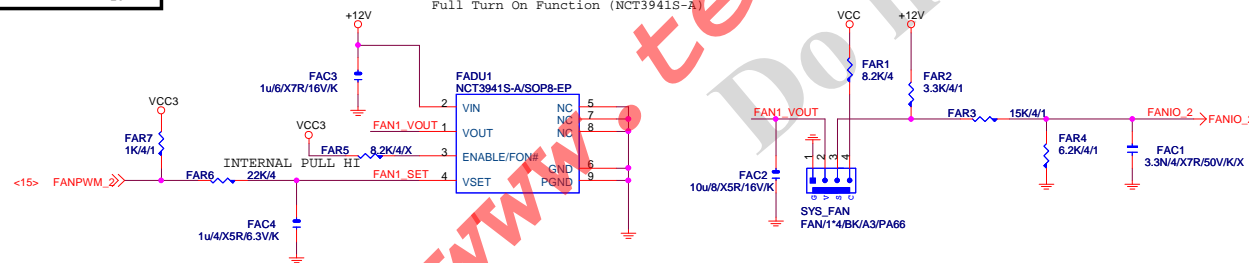
CPU_FAN



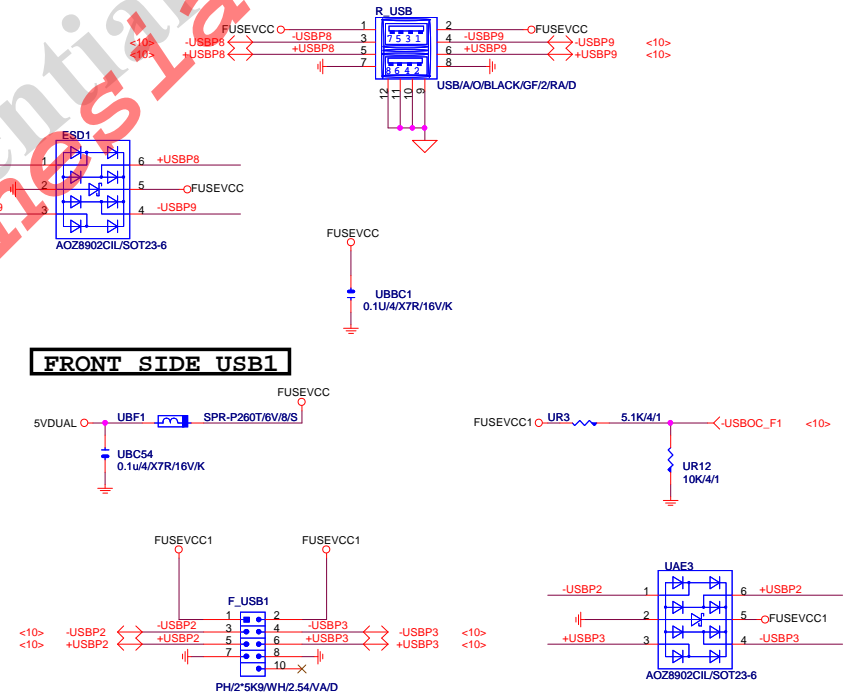
SYSTEM_FAN

Linear SYS_FAN

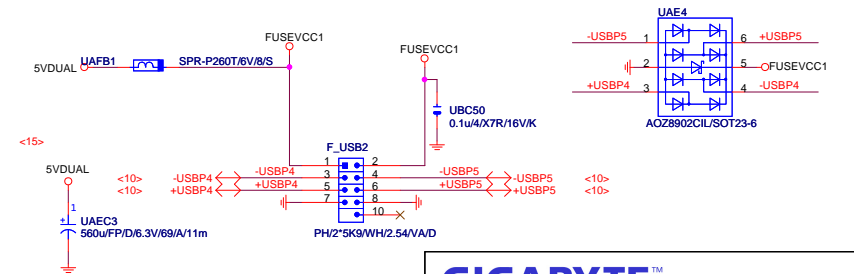
Enable Function (NCT3941S)
Full Turn On Function (NCT3941S-A)



FRONT SIDE USB1



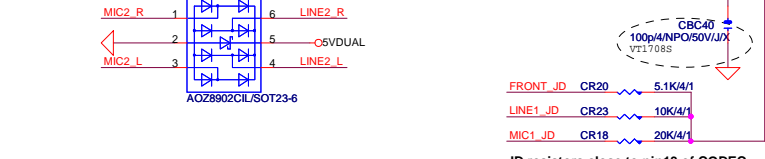
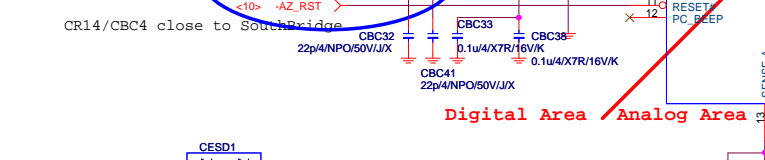
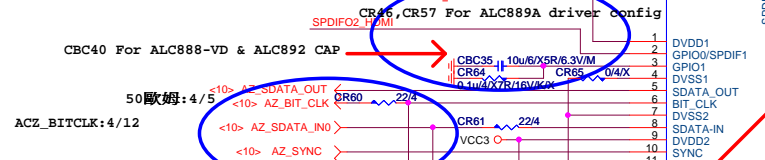
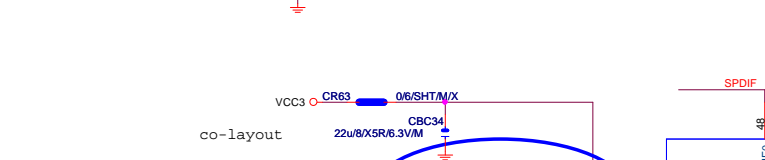
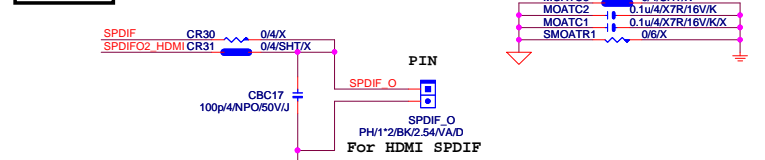
FRONT SIDE USB2



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Title		
FAN , HWMO , R_USB		
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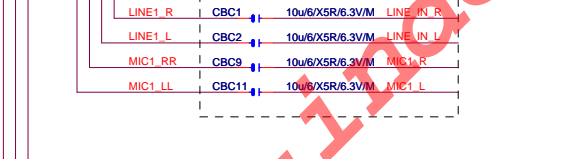
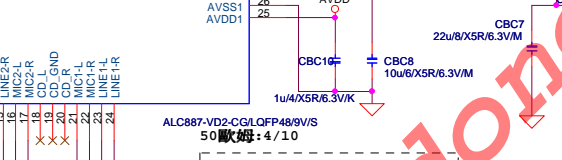
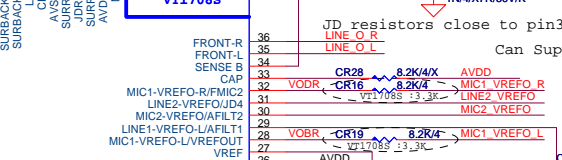
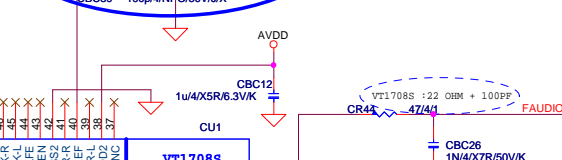
SPDIF_OUT



ALCALIA CODEC

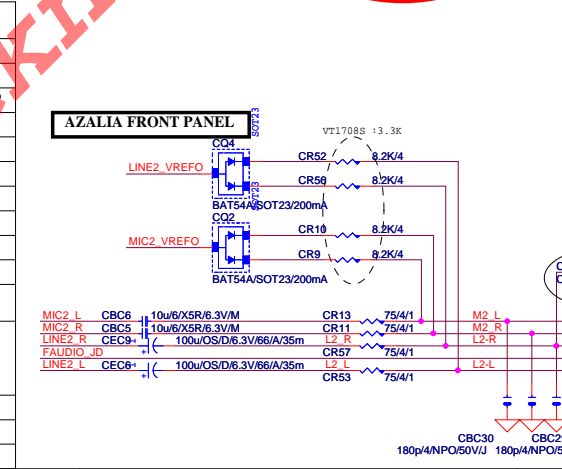
ALC887-VD2/ALC889/VT1708S/VT1708SCE Colay

	ALC887-VD2	ALC889	VT1708S	VT1708SCE
CR65	X	O	O	X
CR64	X	X	X	O
CR44/CBC26	47ohm+1nF	47ohm+1nF	22ohm+100P	22ohm+100P
CR34	20K/1%	20K/1%	5.1K/1%	20K/1%
CR31	O	O	O	O
CR30	X	X	X	X
CBC1/CBC2	22uF/X5R	22uF/X5R	22uF/X5R	22uF/X5R
CR20	5.11K/4/1	5.11K/4/1	5.1K/4/1	5.1K/4/1
CBC35	O	X	X	O
CBC39/CBC40	N/A	N/A	100P/4	100P/4
CR6/CR7/CR54/CR58	22K/4	22K/4	10K/4	10K/4
CR5/CR8/CR13/CR11/ CR57/CR53	75 ohm	62 ohm	75 ohm	75 ohm
CR51/CD1/CBC7	O	X	X	O
CD2/CD3/CQ3/CQ5	X	O	O	X
CR1/CR14/CR17/CR22	75 ohm	62 ohm	1K ohm	1K ohm

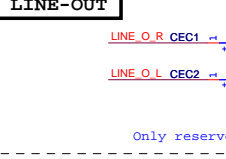
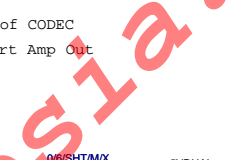
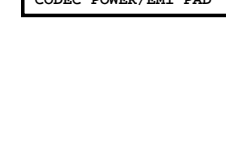


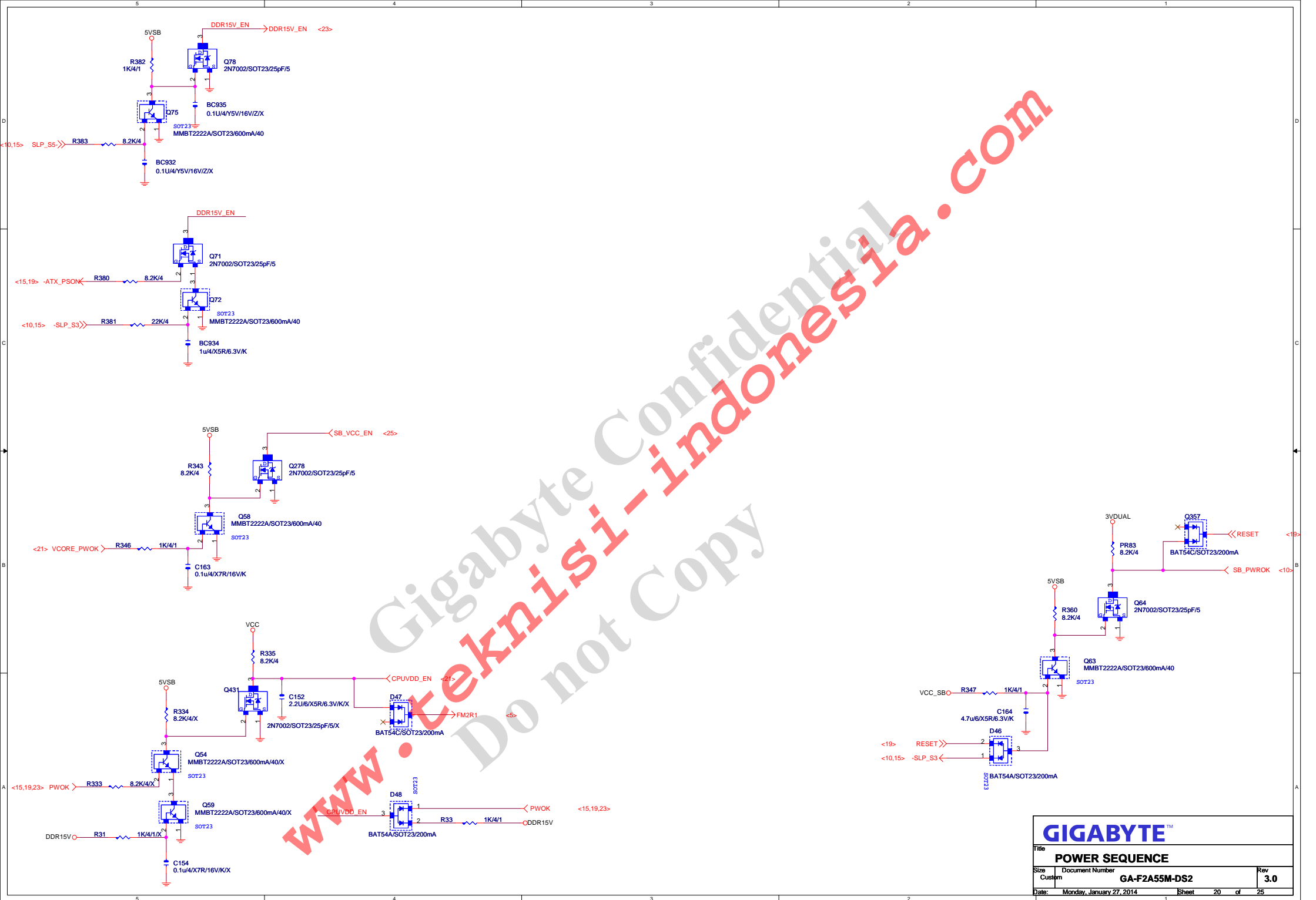
ALCALIA FRONT PANEL

ALC887-VD2/ALC889/VT1708S/VT1708SCE Colay



CODEC POWER/EMI PAD

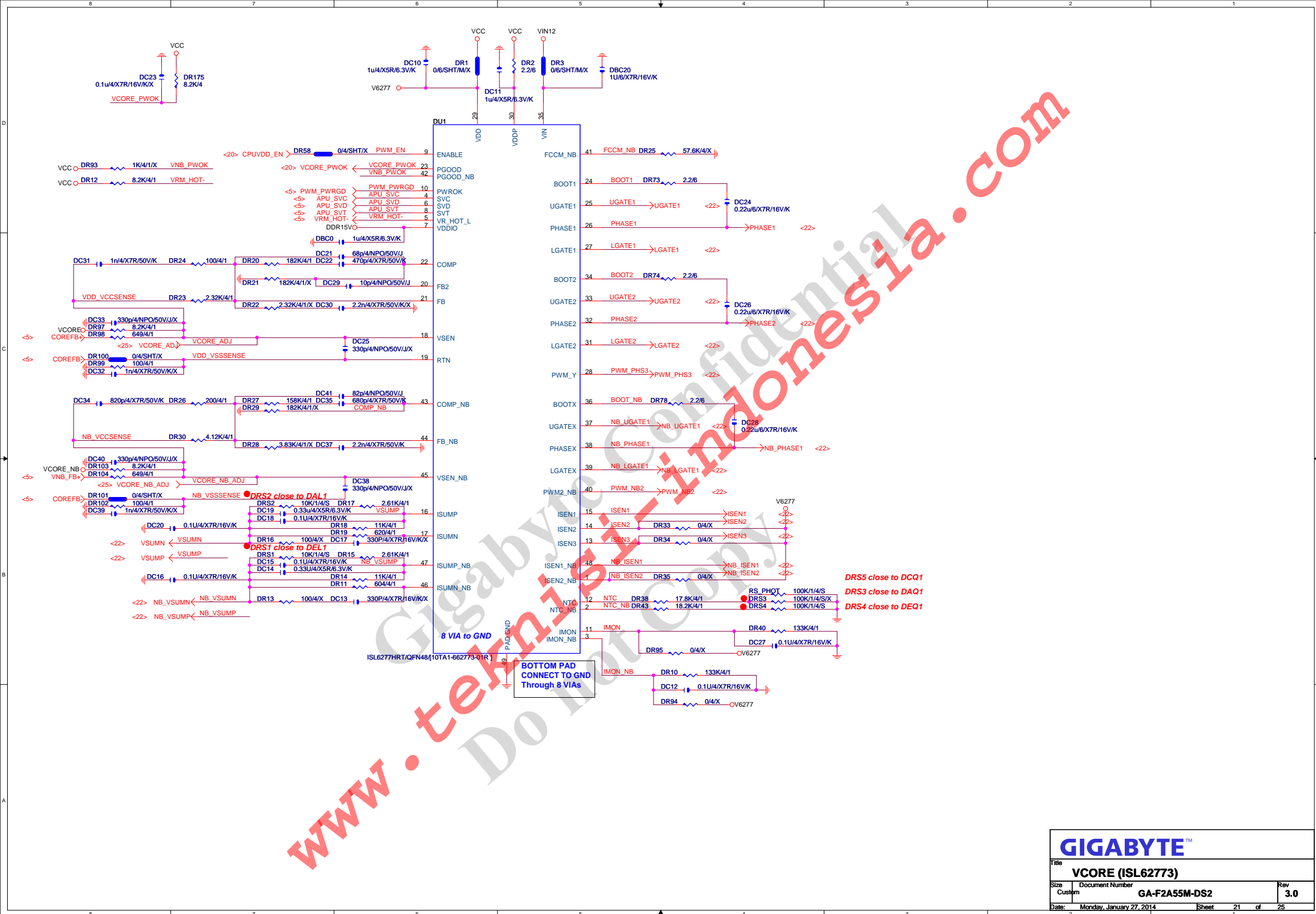


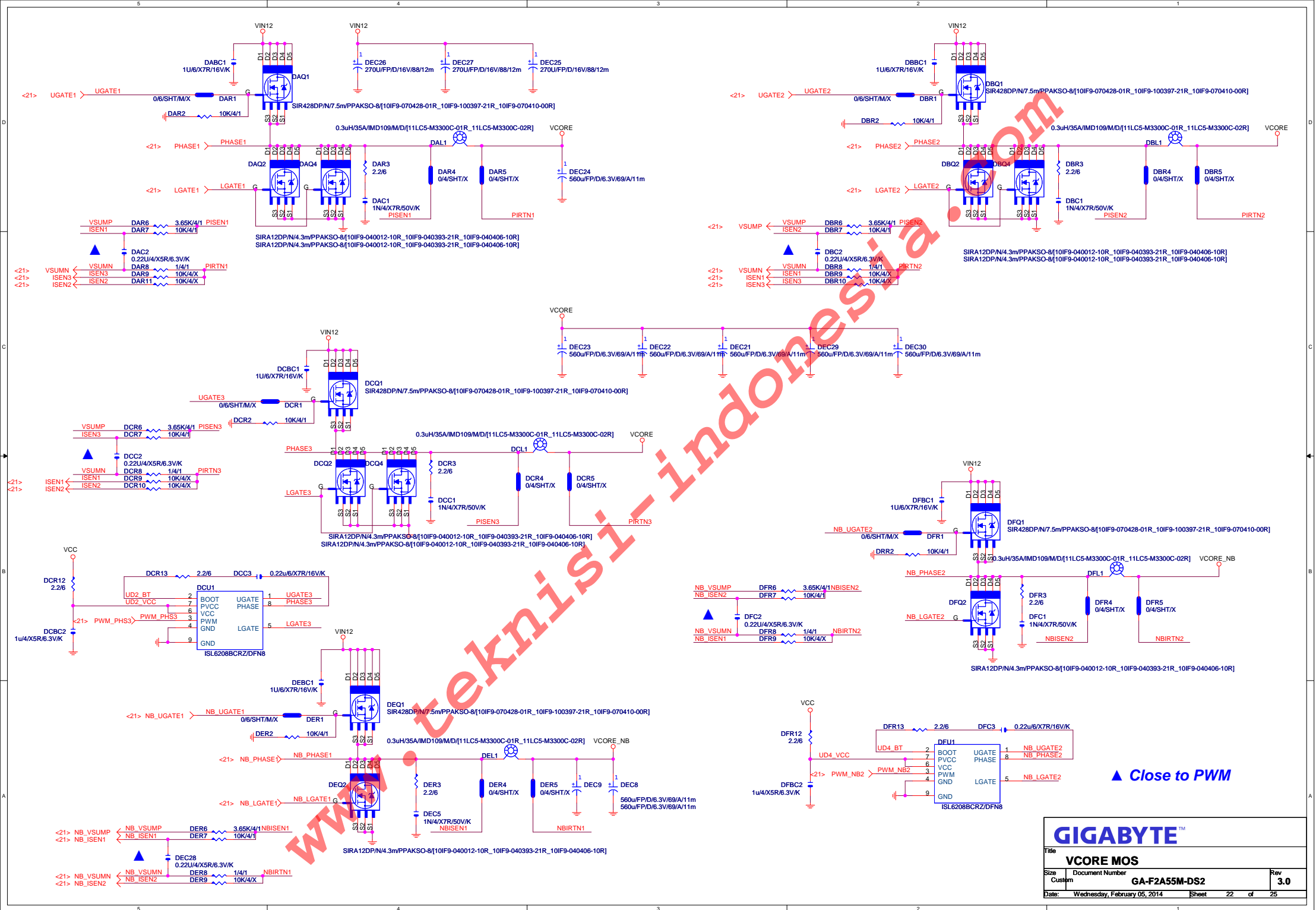


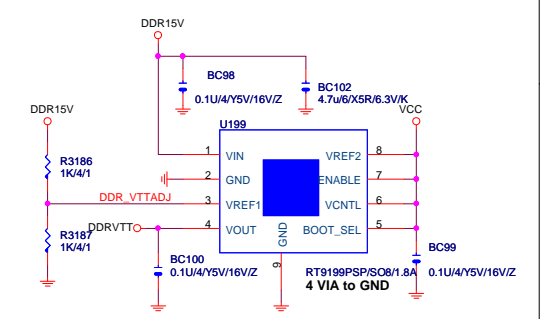
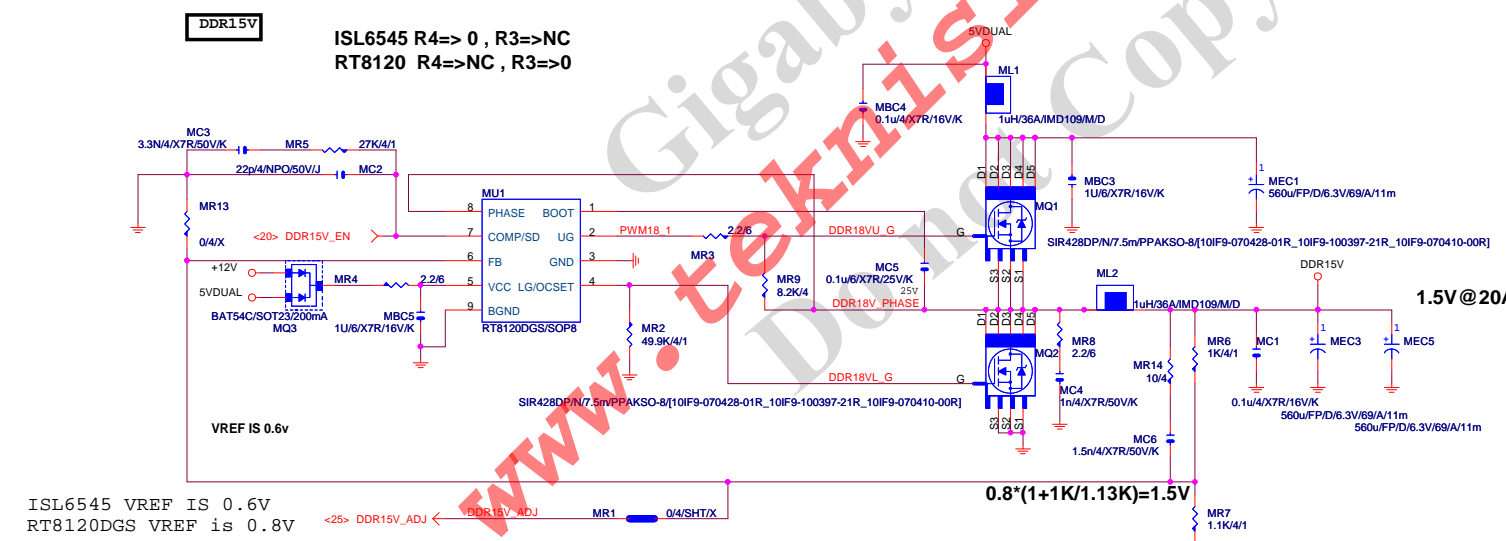
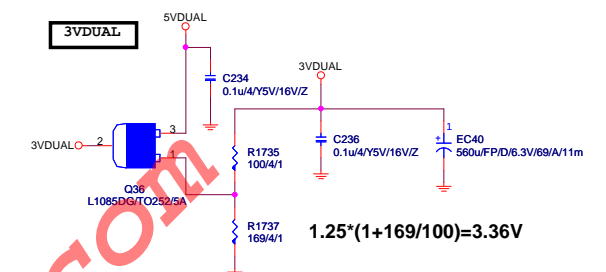
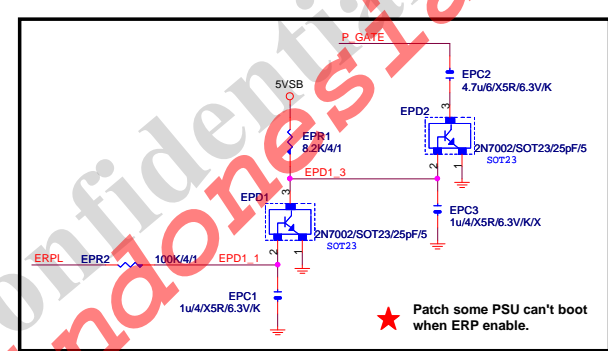
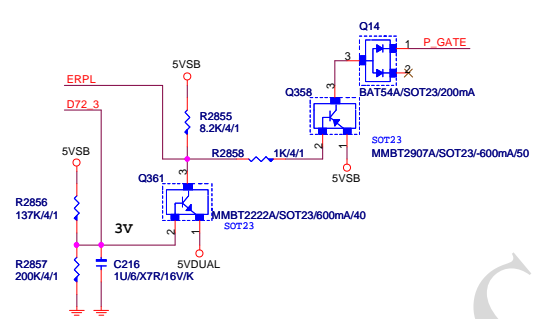
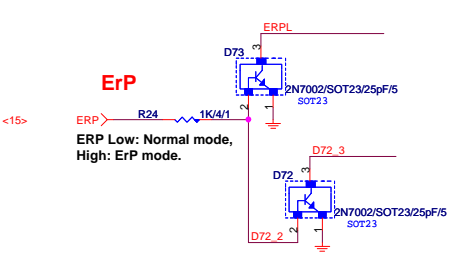
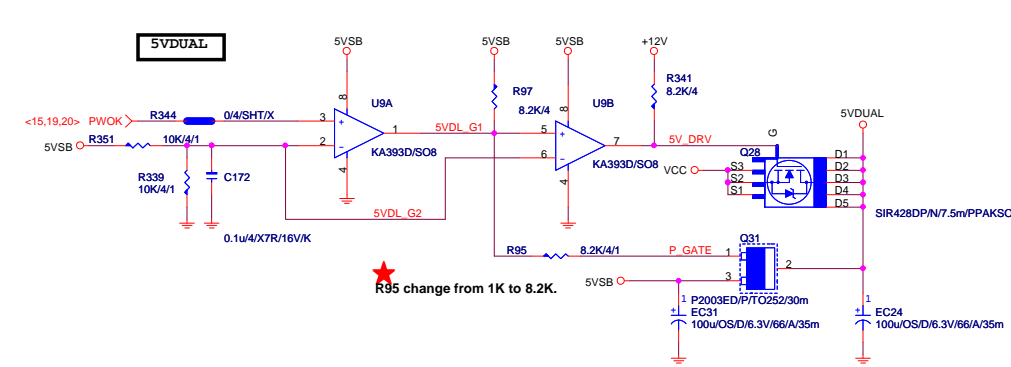
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POWER SEQUENCE

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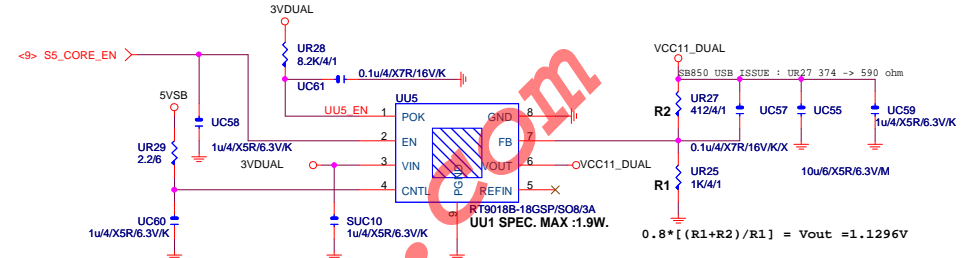
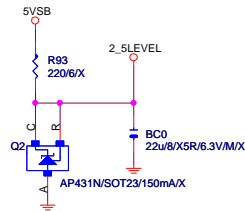
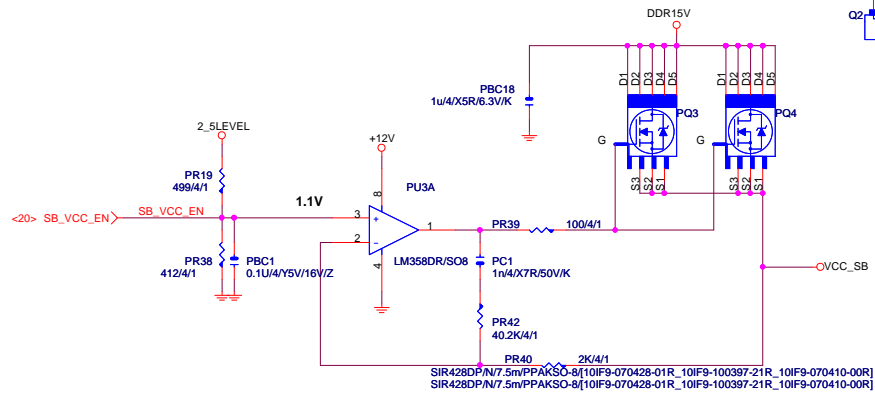


ISL6545 VREF IS 0.6V
RT8120DGS VREF is 0.8V

$$0.8 * (1 + 1K / 1.13K) = 1.5V$$

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Title			
DDR II POWER , VCC18 , ErP			
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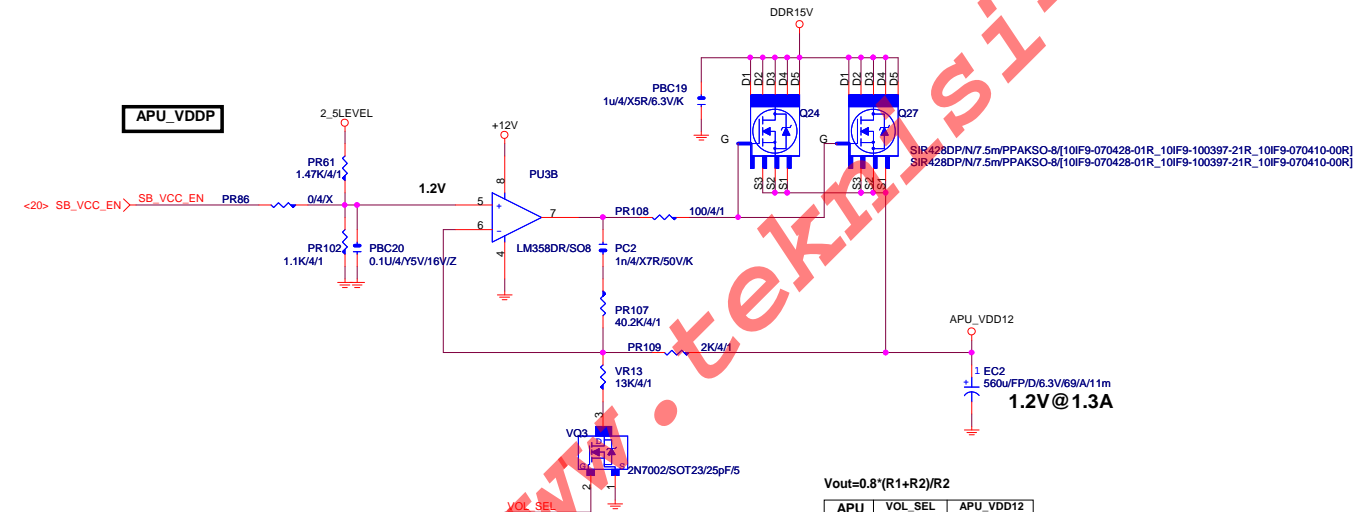
VCC_SB



1.2V@1.69A



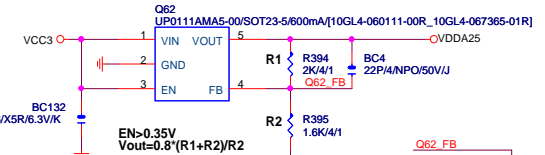
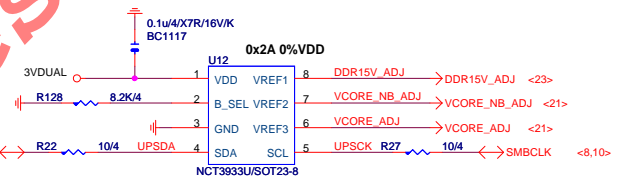
APU_VDDP



1.2V@1.3A

$$V_{out} = 0.8 \cdot (R1 + R2) / R2$$

APU	VOL_SEL	APU_VDD12
FM2	1	1.2V
FM2+	0	1.05V



Max 500mA

APU	VOL_SEL	VDDA25
FM2	1	2.5V
FM2+	0	1.8V

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